BELLCOMM, INC.
955 L'ENFANT PLAZA NORTH, S.W. WASHINGTON, D. C. 20024

SUBJECT: Analysis of the Apollo Entry Monitor System's ΔV Counter Case 320

DATE: April 16, 1969

FROM: D. O. Baechler
R. Lindner, BTL

ABSTRACT

The Apollo Entry Monitor System (EMS) has experienced anomalies during recent Apollo flights and during testing. At the request of NASA-MSC, Bellcomm and Bell Telephone Laboratories examined the logic design of a portion of the EMS--the ΔV counter.

Except for one case, no fan-out limits were exceeded and therefore overall noise margins will be as stated by the integrated circuit manufacturer if the specified supply voltage is provided. Line drivers have been used unnecessarily and, in one case, improperly. This results in unnecessary potential noise sources and, in the case of the improperly used driver, a possible loss of the functions associated with the circuit. The failure to connect unused flip-flop set lines to the supply voltage provides a potential noise pickup problem, the seriousness of which is emphasized by the existence of the unnecessary noise sources. A logic race which occurs can explain one of the observed anomalies only if an unlikely set of conditions exist.

The line driver that is improperly used should certainly be replaced. It is probably impractical to connect the flip-flop set lines to the supply voltage except for newly procured flip-flops, on which the manufacturer can do the connecting. Other steps that can be taken to reduce the noise sensitivity are to insure that specified supply voltage is maintained and to replace 47 line drivers with a regular gate.

A test should be conducted to determine if a logic race is the cause of observed anomalies and if so a change in the logic (one is suggested) should be made to remove the race. Any units that are going to be operated without replacing the improperly used line driver should be tested to see if the functions associated with that circuit are affected.

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MEMORANDUM FOR FILE

I. INTRODUCTION

The Apollo Entry Monitor System (EMS) comprises a scroll assembly which is used to show g's versus velocity during entry and a ΔV counter which is used to display range-to-go to splashdown, range derived from VHF ranging during rendezvous maneuvers, and acceleration in the form of ΔV. The system experienced several observed anomalies in operation during recent Apollo flights and during testing. NASA-MSC assembled a task team to determine the cause and recommend solutions for the anomalies.* Bellcomm and Bell Telephone Laboratories were asked to examine the logic design of the ΔV counter to determine noise margins and to identify noise-sensitive areas in the design.

The ΔV Counter

The ΔV counter is the term used in this report for the part of the EMS that includes the circuitry for counting and interpreting incoming pulses from the EMS accelerometer and displaying the decimal equivalent on a six-digit electro-luminescent (EL) display meter. The EL display has a decimal point between the first and second decades and can have a minus sign in the sixth decade, permitting displays of numbers from -9999.9 to 99999.9. Because a digit is formed by lighting some combination of the seven EL segments in a decade, it is possible to have a failure that results in an unintelligible display.

Depending on the state of external control lines called UP and DOWN, the counter can count up or down from zero or from a number manually set into the counter.

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*"Discussions of Apollo Entry Monitoring System Problems," P. S. Schaenman, February 20, 1969. Bellcomm Memorandum for File, Case 320.

"Meeting on Apollo Entry Monitor System Problems," D. O. Baechler, March 3, 1969. Bellcomm Memorandum for File, Case 320.

On the EMS panel are a mode switch with positions STNBY, AUTO and MANUAL; a function switch with positions EMS TEST 1 through 5, RNG SET, ΔV_o SET, ENTRY, ΔV TEST, ΔV SET, ΔV and OFF; and a ΔV/EMS SET switch with the sequence of positions FAST UP, SLOW UP, OFF UP, OFF DOWN, SLOW DOWN, and FAST DOWN. Figure 1 shows the EMS panel with the scroll assembly removed.

Fault History

Significant faults that have been observed are as follows:

1. On CSM 101 (Apollo 7) the counter jumped to 90000.0 during preflight, flight and postflight use.

2. On CSM 103 (Apollo 8) the counter jumped to -100.4 at S-IVB separation; during mid-course correction (MCC) No. 5, the velocity went negative instead of stopping at zero; and after MCC No. 5 the counter jumped to various values when an astronaut manipulated the mode and function switches to try to pinpoint the problems he had experienced.

3. Some counter segments lighted during tests on CSM 106 when cabin lights were turned on.

4. During CSM 111 vibration tests, the counter jumped to 99999.9 on one occasion, on another occasion it reset to zero when it was not supposed to do so, and on a third occasion the V_o initialization was improper.

In addition to these counter problems, the scroll unit exhibited scribe perturbations during CSM 103 entry.

Autonetics* has given the following explanations for these faults:

1. The jump to 90000.0 was caused by intermittently increasing resistance through a crimped connector--that is, a loose connection. Further study showed increased crimp joint resistance with age. Specific effect of time on resistance is not known, but all units that are potted and aged show a voltage drop across the crimp joint of 0.05 volt to 0.75 volt with

*Autonetics Division, North American Rockwell Corporation, is the manufacturer of the EMS.

an average of 0.20 volt. The jump to 90000.0 was caused by a combination of a worst case transistor in the sixth decade and the reduced collector voltage.

2. The counter jump to -100.4 was caused by a logic peculiarity coupled with (a) the counter being at zero and (b) two $-\Delta V$ pulses from the accelerometer being followed by one $+\Delta V$ pulse. The jumps during and immediately following MCC No. 5 were the result of bubbles in the accelerometer. These bubbles also caused the scribe perturbations during entry.

3. Counter segment lighting during CSM 106 testing was the result of poor workmanship in wire routing.

4. The counter jump to 99999.9 was caused by logic peculiarities. The reset to zero and V_o initialization problems were a result of switching transients.

Autonetics has suggested the following corrective actions to overcome these problems:

1. Since the crimp connectors don't exhibit high resistance when new, low voltage screening of new units will show up marginal units.

2. Logic peculiarities won't cause problems if ΔV is monotonically changing as it does when the EMS is used for ΔV, VHF ranging and entry range-to-go. For any other use, a procedural change to bias the counter away from zero should be initiated. A screening test for bubbles will eliminate problems caused by the accelerometer bubbles.

3. Poor workmanship will be corrected by more testing.

4. Procedural changes will halt the effects of the logic peculiarities. No switching transients will occur if the EMS is used in accordance with Apollo Operations Handbook procedures.

Scope of Study

The false jumps believed to be caused by logic peculiarities and switching transients are the topic of this study. Three characteristics of the EMS design were studied in an

effort to detect the cause of the jumps. They are the logic peculiarity or logic race, the application of line drivers, and the hook-up of flip-flops. Integrated circuit loading limitations were reviewed. None of the discrete devices--transistors, diodes, SCR's and their associated circuitry--were included in the study.

II. LOGIC RACE PROBLEMS

Propagation Delay Times

The detailed analysis of a logic race required knowing the values of turn-on and turn-off propagation delay times. This information was available* as the maximum values for both a fan-out of one and a maximum fan-out. For fan-outs between the extremes it was necessary to use interpolation. Later information was obtained** concerning minimum values but only for a fan-out of one for turn-on and maximum fan-out for turn-off. Typical values and distributions were not available.

The Autonetics specifications were not used for this study since only limits for maximum fan-out were given, although a fan-out of one is by far the worst case for turn-off delay. It was also noted that the limits stated in the specifications for maximum fan-out are in general looser than those published by Signetics.

A Fault-Causing Race

The logic involved in accepting pulses from the accelerometer and translating them to a digital display is shown in Figure 2. The figure shows only those gates necessary to explain the logic race. The gate designations are the same as those used on Autonetics drawings 40815, 40832, and 40831.

A situation that could cause a false jump has been described by R. A. Harris of Autonetics and is shown in the timing diagram of Figure 3. Starting from an all zero condition in the display, two $+\Delta V$ pulses are followed by a $-\Delta V$ pulse resulting in the backward enable signal being still high when a clock pulse arrives at the backward transfer gate. Since the output of the backward transfer gate is interpreted as a count pulse in the next decade, subsequent decades may count to nine.

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*SE100J-SERIES Design and Applications, June 1966. Signetics Corporation.

**Telephone conversation between R. Lindner and Mr. Les Brock, Applications Engineer, Signetics, Inc. March 11, 1969.

This situation has been examined in greater detail by using maximum propagation delay times. Starting with t=0 at the leading edge of the $-\Delta V$ pulse and using the same logic states as in Figure 3 up to that time, the pulse times are recorded in Figure 4 for each point in the logic. In particular, it can be seen in Figure 4 that because of unequal gate delays from $-\Delta V$ to the UP and DOWN points, a 125ns negative going pulse is found at the output of gate 2C. Then since the COUNT pulse has arrived at gate 4A before this, a short pulse preceding a slightly shortened 7.5μs pulse is caused at the input to the one shot. This short pulse falls to zero at 231ns, triggering a one shot pulse at 266ns. The pulse from the one shot is inverted by gate 1A to become a positive clock pulse for both the counter flip-flops in decade 1 and the transfer gates to decade 2. This is an unwanted or false pulse. However, since the clock pulse must charge a 70pF capacitor at each flip-flop, the switching delay of gate 1A can be 90ns, giving a time of 356ns before the clock pulse can reach the backward transfer gate 12B.

During this time the COUNT pulse has also proceeded through the gated flip-flop formed by gates 10A, 10B, 10C, and 6D. (The zero sense line is high.) Also since the flip-flop 3 is set (Q=1), the backward enable gate 18A should go low at 258ns. Thus the backward enable and the clock are typically not both high which would make it impossible to gate a false transfer pulse through gate 12B. The equations are as follows:

TIME - PROPAGATION, HIGH TO LOW (BACKWARD ENABLE TO ALL DECADES); $t_{PHL}(BE)$

$= t_{ON}(13C + 4A + 10A + 10C + 18A) + t_{OFF}(20B + 4C + 6D + 12D)$

$= 18 + 17 + 17 + 19 + 15 + 32 + 50 + 40 + 50 = 258ns$

TIME - PROPAGATION, LOW TO HIGH (CLOCK TO DECADE 1), $t_{PLH}(C1)$

$= t_{ON}(13C + 18B + 2C + 4C + 7) + t_{OFF}(15C + 2A + 4A + 1A)$

$= 18 + 13 + 17 + 18 + 35 + 55 + 50 + 60 + 90 = 356ns$

TIME - PROPAGATION, LOW TO HIGH (CLOCK TO DECADE 2), $t_{PLH}(C2)$

$= t_{PLH}(C1) + t_{ON}(12A) + t_{OFF}(1A)$, if $t_{PHL}(BE) > t_{PLH}(C1)$

$= 356 + 13 + 90 = 459ns.$

The equations can be used with different delay times to check if $t_{PHL}(BE) > t_{PLH}(C1)$ which can produce a -9.2 display or if $t_{PHL}(BE) > t_{PLH}(C2)$ which can produce a -99.2 display. But using the above values, the margins against these occurrances are 98 and 201ns respectively.

As mentioned, Signetics has provided some data for worst case minimum delay times. Using both maximum and minimum limits, it is possible to assign to each gate the delay time that makes the race condition most likely to produce spurious numbers. This absolute worst case results in about a 70nsec margin in favor of the spurious number -9.2 appearing (25nsec in favor of -99.2).

In order to explain how the -100.4 jump may have occurred, another situation was suggested by Autonetics. To describe it, the longer time scale of Figure 5 is needed. In this figure, assuming $t_{PHL}(BE) = 500ns = 0.50\mu s$, all the pulses indicated by the solid lines would occur and the display would be -99.1 after 5.3μs and -99.2 after 12.8μs. The dashed lines represent the pulses if the following situation occurred. The S_c line of flip-flop E is low for a period of time (∿.2μs) while the clock is high. From the time 0.56μs this S_c line goes high causing its R_c line to go low. Then at 5.28μs the clock goes low, triggering flip-flop E. The result should be that E remains zero. If, however, the charge on the set capacitor has not leaked off in this 4.72μs period (it should discharge in 2.2μs) the trigger would find both set and reset capacitors charged, resulting in an indeterminent condition. If the less likely result prevailed, flip-flop E could set. This would then cause a forward transfer pulse at gate 12B at the time 5.4μs. The display would now be -99.(AE) after 5.3μs and -100.(B) after 12.8μs. The (AE) and (B) represent scrambles since they are not number codes.

It is also of interest to note the result of succeeding -ΔV pulses. Some of that list is shown below.

FALSE PULSE	-99.(AE)	or	-99.□
PULSE 1	-100.(B)	or	-100.■

PULSE 2	-100.(AC)	or	-100.4
PULSE 3	-100.(ABD)	or	-100.4
PULSE 4	-100.(ABCE)	or	-100.4
PULSE 5	-101.(BCD)	or	-101.4

The display -100.4 cannot occur with additional $-\Delta V$ pulses. In fact, pulse 5 advances the counter to -101.

Check for False Backward Transfer

The actual values of $t_{PHL}(BE)$, $t_{PLH}(C1)$, and $t_{PLH}(C2)$ on an existing EMS can be checked on an oscilloscope. Probes should be connected to the backward enable (lead 3 of 40831) and the output of EZ1A of 40831 in decades 1 and 2. In a potted unit the output of EZ1A is probably not available. The closest point would be the input of EZ1A (lead 14 of 40831 on decade 1) which would differ by the turn-off delay of EZ1A which is 40 to 90ns. Also the backward transfer output (lead 1 of 40831) on decades 1, 2 and even 3 should be monitored.

The result of this test would be to find out whether the false transfer takes place in a particular EMS and to determine the time margin for or against its taking place.

If the oscilloscope measurements show that the false transfer takes place, the short term solution is certainly to bias away from zero. If a long term solution is desired, the next section describes two methods which involve logic changes. But without the oscilloscope proof, the suggested long term solutions become academic.

Elimination of False Pulse

A way of eliminating the false pulse (which will assuredly prevent false transfers) by adding gate delays in the COUNT line just after the 20B gate was suggested by Autonetics. Referring back to Figure 4, if the COUNT pulse transition from low to high was delayed from t=50ns to after 153ns, the output of gate 4A would remain high until 295ns and would not show the extra pulse. It would be necessary to insert well over 103ns of delay to prevent the false clock pulse. This would require at least six gates. Of course, there would still be a race, only the false pulse would not normally occur.

An alternate solution is to remove gate 2C, thereby eliminating the false pulse by eliminating the race. Gate 2C inhibits the count gate 4A when neither the UP line nor the DOWN line is high, so if it is removed the inhibit input to gate 4A must be provided in some other way.

The only time gate 2C is supposed to have a zero output is when the function switch is set to either V_o SET, RTG SET, ΔV SET, TEST 1, TEST 2, or TEST 3 and the slew switch is not in the FAST or SLOW UP nor the FAST or SLOW DOWN position.

One method of accomplishing this is shown in Figure 6. Two expander gates (one package) have been added. The expander on EZ8B frees gates EZ8A and EZ7C. Then EZ8A is used with an expander to yield the function

$$EZ8A = \overline{SET} + FAST\ UP + FAST\ DOWN + SLOW\ UP + SLOW\ DOWN$$

where

$$SET = V_oSET + TEST1 + TEST2 + RNG\ SET + \Delta V\ SET + TEST3$$

Gates EZ7C and EZ2C are not used.

Since this inhibiting signal is a function only of switch positions, it is not subject to faults caused by changes in $+\Delta V$ and $-\Delta V$ pulses. There are, of course, other similar methods that could be used. The particular method should be chosen by someone intimately familiar with both the logic design and operation of the EMS.

Minor Race Problem

In normal operation the flip-flop 3 clocks on information obtained from the previous pulse. Thus when the acceleration changes sign, the first pulse is counted in the wrong direction. Autonetics recognizes this was a design error but feels it can be accepted since it only results in a 0.2 ft/sec error. It can be shown using delay times obtained from the Signetics booklet that changing from $-\Delta V$ to $+\Delta V$ the clock pulse arrives 73ns too soon at flip-flop 3 and when changing from $+\Delta V$ to $-\Delta V$ it arrives 150ns too soon. Delay in the COUNT line as suggested for the other race problem would also prevent counting the first pulse in the wrong direction but a delay of well over 150ns or about ten gates would be needed. The suggested change in gate 2C does not eliminate this minor race problem.

III. EFFECT OF VHF RANGING

For CSM 106 VHF ranging can also use the same counting logic. As shown in Figure 7, if either X_{11} or X_{MAN} is high, the VHF logic is simply a pair of gates inserted at the COUNT, UP and DOWN points of Figure 2. The false pulse will still occur and the jump to -99.2 or -100.(B) still should not (but might) occur. In fact, due to the slight difference in delay through gates 5A and 9A of Figure 7, compared to that of gates 5B and 10A, the margin against false backward transfer is increased from 98ns to 122ns.

At the bottom of Figure 7, the VHF logic is shown for the case when VHF ranging is being done. Figure 8 shows the appropriate pulse trains. The VHF data was assumed to be amplitude modulated but frequency modulation could as well be assumed. The down count command would forward enable the counter for almost 100μs. Since the UP pulse goes low before the DOWN pulse goes high, gate 2C of 40832 does not go low. Also, the one shot 6 delays any COUNT pulse for 6.8μs. Either fact is sufficient to prevent a false clock pulse. In addition, flip-flop 3 now clocks on the present down count command, assuming the command came at about the same time as the VHF data.

Another minor race problem consists of the race between the outputs of flip-flop 3 and the output of gate 4C to reach gates 10A and 10B. The pulse from 4C should arrive 48ns before $\overline{Q}$ goes low. This will turn on the minus sign and the counter will forward enable. If $\overline{Q}$ is still high when the pulse from 4C goes high the counter will lose two counts just as it did in the other minor race problem. However, unlike the other minor race, this race normally results in a correct output. Also, this race has no effect unless the counter is at zero, so that the ALL DECADES ZERO SIGNAL is high.

IV. USE OF DRIVER GATES

A commonly used gate in the EMS is the SE156J driver gate. This gate has an active pull-up due to transistor T_3 in Figure 9. An active pull-up is necessary when driving lines with a large capacitive load. However, the active pull up also makes the gate a potential noise generator due to internal timing differences. Thus, when using the gate it is recommended practice to have a by-pass capacitor from V_{CC} to ground, connected close to the package. Also, when there is no capacitive load there is no need for the active pull-up driver and it should not be used.

In the EMS, the SE156J (477-0163-001) dual driver package is used 70 times with a total of 138 drivers connected. Six drivers (EZ1A of 40831) are certainly used properly as they must drive five clock inputs. Twenty-five others are used with high fan-out but not high capacitance. This could have been done with the SE111J which is a high fan-out gate without an active pull-up. Another 24 drivers were used only for their fan-in capability. Here the SE116J would have been the better choice. Both the SE111J and the SE116J have the same pinning as the SE156J. Finally, 32 drivers are used neither for fan-in nor fan-out but simply because they are available. The remaining 51 drivers are used for test positions or decoded outputs for which use an active pull-up driver is probably unnecessary but is considered as unknown. The complete list of packages and their loading is shown in Table 1.

Due to practical problems of package layout and device qualification it would seem adviseable to recommend the replacement of only 24 of the SE156J packages. These packages are the ones in which neither driver is used for high fan-out and are indicated in Table 1. The replacement is the SE116J which as mentioned has the same pin designations and thus is a simple one-for-one replacement.

The replacement of one of the drivers, EZ14 of 40815, is most necessary as explained in the next section.

Effect of Collector Logic Using Driver

It is not allowable to use collector logic, that is, to wire the outputs of two or more gates together when using an active pull-up driver as one of the gates. Unfortunately, this was done with the outputs of the driver EZ14A and the gates EZ13B, 16A, and 16B of 40815. The affected circuitry is shown in Figure 10. The connected outputs drive an input of the EZ20B which gates the COUNT pulse. When counting from accelerometer pulses, as in Figure 2, there is no problem since all four of the gates with connected outputs are off ("one" state). However, if one of the gates is on while the driver gate and the other two gates are off, a very serious condition exists. The current paths are shown in the bottom half of Figure 10.

The result is that the on-gate (13B as shown) must saturate over 30mA when its normal maximum is 12mA. Or in other words, the effective fan-out of this gate is about 27 while it is rated at 6. In fact, the gate will probably work under this condition near room temperature although it will turn on much slower than specifications and have a much lower noise margin.

If in some EMS the reduced margins are exceeded, the consequence would be a loss of one or more functions that rely on turning on gate 13B, 16A or 16B. For instance, if gate 13B could

not turn on, it would not be possible to slew the counter FAST UP or FAST DOWN with the function switch in the RTG SET, ΔV SET or TEST G < 0.2 positions--SLOW UP and SLOW DOWN would work because they go through driver 14A. If gate 16A could not turn on, then with the function switch at ΔV TEST and the mode switch at AUTO, the expected ten seconds of +ΔV pulses would not be counted. If gate 16B fails to turn on, then with the function switch at ΔV and the mode switch at MANUAL, no +ΔV pulses would be counted. None of these symptoms have been observed, but it is possible that, for instance the FAST UP failure could go unnoticed if it failed at the first manipulation of the slew switch and operated subsequently. And if the function switch is at ΔV and the mode switch at MANUAL, it may not be apparent that the lack of count pulses is due to a failure instead of the absence of +ΔV pulses. Because of these considerations, the driver EZ14 of 40815 should certainly be replaced with an SE116J package.

V. EFFECT OF NOISE ON FLIP-FLOP

It is recommended practice to connect unused direct set and reset inputs of the SE124J flip-flop to V_{cc}. This is done to prevent r-f pickup which could falsely change the flip-flop state. This was not done in the EMS. However, it was learned that the unused package leads were clipped at the glass edge which should reduce the antenna effect.

Of the 128 flip-flops used in the EMS, 103 have unconnected S_D or R_D inputs or both. However, due to practical considerations it is probably impossible to connect them to V_{cc} at this time. Perhaps a high frequency mica bypass capacitor from V_{cc} to ground associated with each decade counter would help.

Of particular concern is the fact that the direct set leads of the decade counter flip-flops are unconnected and that this input is adjacent to the ground lead. If a fast rise time noise pulse occurred on the ground line it could cause a flip-flop to set. And the setting of a single flip-flop (flip-flop A of decade four) due to a noise pulse could give a 100 in the display. The observed 100.4 could have resulted from such an occurrance followed by four true counts.

Overall System Noise Margin

All the 325 integrated circuits in the EMS were examined for fan-out. Such recommended additions as 3/4 load for an added connected output, one extra load for an R_C or S_C input, an extra half load for a clock input, and an extra four loads for a one shot pull-up resistor were used.

Except for the error in using a driver for collector logic, no fan-out limit was exceeded. The maximum fan-out for a gate was 5 (6 is allowed), for a driver 15 (19 is allowed), for a flip-flop 6 (7 is allowed), and for a one shot 5 (5 is allowed).

Thus if 4.0 ± 0.4V is applied to the integrated circuit packages and if the temperature is not far from 25°C the worst case noise margin will be as stated by Signetics. These values are 1.2V high level DC margin and 0.85V low level DC margin.*

An exception to the above is when expanded gate elements are used to increase the fan-in. This happens five times in the EMS and is perfectly legal as long as the expander package is at the same temperature as the expanded gate. However, according to Signetics the noise margin for seven added diodes, which is the most in the EMS, is 1.03V high level DC margin and 0.643V low level DC margin.

High level noise margin varies with supply voltage but low level noise margin is not affected appreciably at 25°C until the supply drops below 3.0V. However, at about 2.5V the low level margin (as well as high level) will drop to zero.

VI. SUMMARY

Four conclusions result from this study to determine the cause of false jumps in the ΔV meter of the EMS. First, there is a logic race that produces a false clock pulse. It is theoretically unlikely that this pulse will cause jumps to 9.2, 99.2 or any of the other jumps that have been observed. Therefore, the pulses should be checked on an oscilloscope to determine if these observed jumps are in fact caused by an unlikely set of circumstances.

Second, line drivers with their potential for noise generation are misused in at least 56 places. Of these, 47 (24 packages) could be easily replaced with a gate. In addition, collector logic with a driver results in a possible loss of some functions. These functions should be carefully tested on existing units.

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*"Worst Case System Design with Signetics SE100J-Series," Signetics, Inc., December 1965.

Third, the flip-flop packages do not have their direct set and reset pins connected to the supply voltage, so that there may be a-c coupling to these lines. Even though they have been clipped at the case it is an undesirable situation that is aggravated by the fact that the direct set line is adjacent to the ground line and it is on the ground line that the drivers have a tendancy to generate noise.

Fourth, except for the one misused driver, no loading limitations on the integrated circuits are exceeded.

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1031-DOB
BTL-RL--jdc

Attachments
Table 1
Figures 1 thru 10

TABLE 1

USE OF BUFFERS (447-0163-001)

GATE NUMBER		FAN-IN	FAN-OUT	COMMENTS	RECOMMEND USE OF SE116J
Schematic No. 40815, Module and Component Assy Electronics					
EZ1	A	2	1	NG	Yes
	B	4	2	NG--Used for fan-in	
EZ8	A	3	5	NG	Yes
	B	3	4	NG	
EZ14	A	4	3 1/4	Disaster--Output "OR"ed	Yes
	B	4	1	NG--Used for fan-in	
EZ17	A	2	3	NG	Yes
	B	1	3	NG	
EZ18	A	2	3	NG	Yes
	B	4	3	NG--Used for fan-in	
EZ19	A	1	1	NG	
	B	1	TEST		
EZ20	A	1	TEST		
	B	4	3	NG--Used for fan-in	
Schematic No. 40832, Counter-Control					
EZ1	A	3	1	NG	Yes
	B	3	1	NG	
EZ8	A	4	8	Proper use	
	B	3	7	"	
EZ9	A	2	7	"	
	B	1	6	"	
EZ13	A	2	1	NG	
	B	1	Relay Driver	Proper use	

Table 1 (Contd.)

GATE NUMBER		FAN-IN	FAN-OUT	COMMENTS	RECOMMEND USE OF SE116J
EZ14	A	2	14	Proper use	
	B	2	14	"	
EZ15	A	2	14	"	
	B	2	14	"	
EZ16	A	4	3	NG--Used for fan-in	
	B	1	10	Proper use	
EZ17	A	1	11	"	
	B	1	10	"	
EZ18	A	2	14	"	
	B	2	14	"	
EZ19	A	1	Decimal Driver	"	
	B	1	6		
Schematic No. 40831, Decoder/Counter (6)					
EZ1	A	2	7	Proper use	
	B	7	Decoded Output		
EZ12	A	4	1	NG--Used for fan-in	Yes (6)
	B	4	1	NG--Used for fan-in	
EZ16	A	3	Decoded Output		
	B	5	"		
EZ17	A	4	"		
	B	3	"		
EZ18	A	2	"		
	B	4	"		

Table 1 (Contd.)

GATE NUMBER		FAN-IN	FAN-OUT	COMMENTS	RECOMMEND USE OF SE116J
Schematic No. 40923, Pulse Scaler					
EZ2	A	1	9	Proper use	
	B	8	1	NG--Used for fan-in	
EZ9	A	2	2	NG	Yes
	B	1	1	NG	
Schematic No. 40906, Master Clock					
EZ19	A	1	1	NG	Yes
	B	1	2	NG	
EZ21	A	1	2	NG	Yes
	B	1	1	NG	
EZ22	A	1	1	NG	Yes
	B	1	1	NG	
EZ23	A	1	1	NG	Yes
	B	1	3	NG	
EZ24	A	1	1	NG	Yes
	B	1	1	NG	
Schematic No. 40854, Control/Divider - Range Integrator					
EZ1	A	1	6	Proper use	
	B	1	13	"	
EZ8	A	7	1	NG--Used for fan-in	Yes
	B	3	2	NG	
EZ11	A	1	14	Proper use	
	B	1	14	"	
EZ12	A	1	14	"	
	B	1	15	"	
EZ26	A	1	1	NG	Yes
B not used					

Table 1 (Contd.)

GATE NUMBER		FAN-IN	FAN-OUT	COMMENTS	RECOMMEND USE OF SE116J
Schematic No. 40889, Detector, 0.2G					
EZ1	A	4	1	NG--Used for fan-in	Yes
	B	4	1	NG--Used for fan-in	
Schematic No. 40926, Detector, 0.05G					
EZ3	A	6	2	NG--Used for fan-in	
	B	3	2+TEST		
EZ4	A	3	1	NG	
	B	3	TEST		
Schematic No. 40911, Time Delay					
EZ2	A	3	14	Proper use	
	B	1	2	NG	
EZ12	A	4	3	NG--Used for fan-in	Yes
	B	1	1	NG	
Schematic No. 40932, Invertor					
EZ10	A	3	TEST+SI+3		
EZ12	A	1	TEST+SI		
	B	1	TEST+SI		
EZ13	A	1	TEST+SI		
	B	1	TEST+SI		
Schematic No. 41057, VHF Ranging					
Z3	A	2	6	Proper use	
	B	2	1	NG	
Z9	A	2	2	NG	Yes
	B	2	1	NG	
Z10	A	2	1	NG	Yes
	B	2	1	NG	

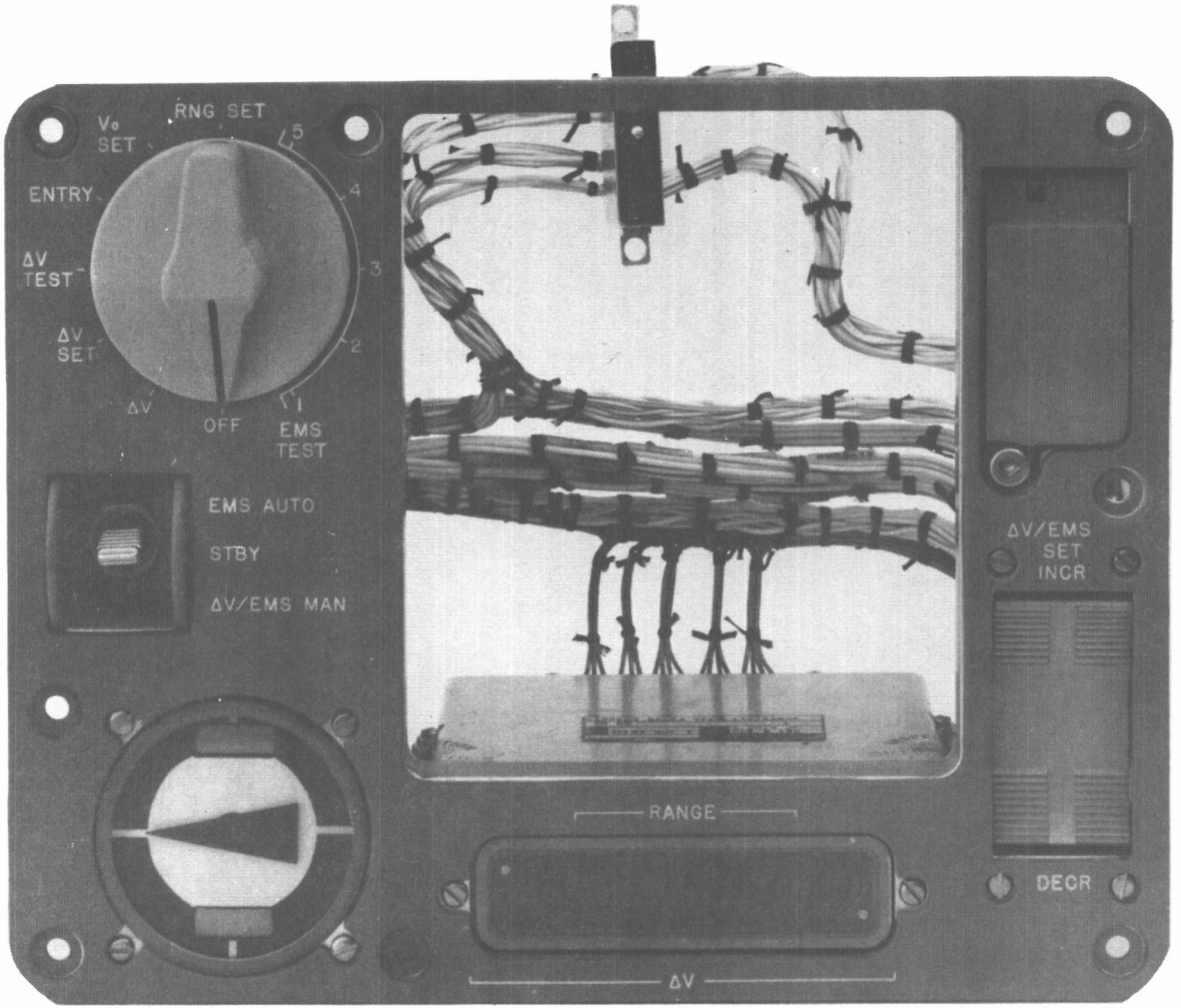
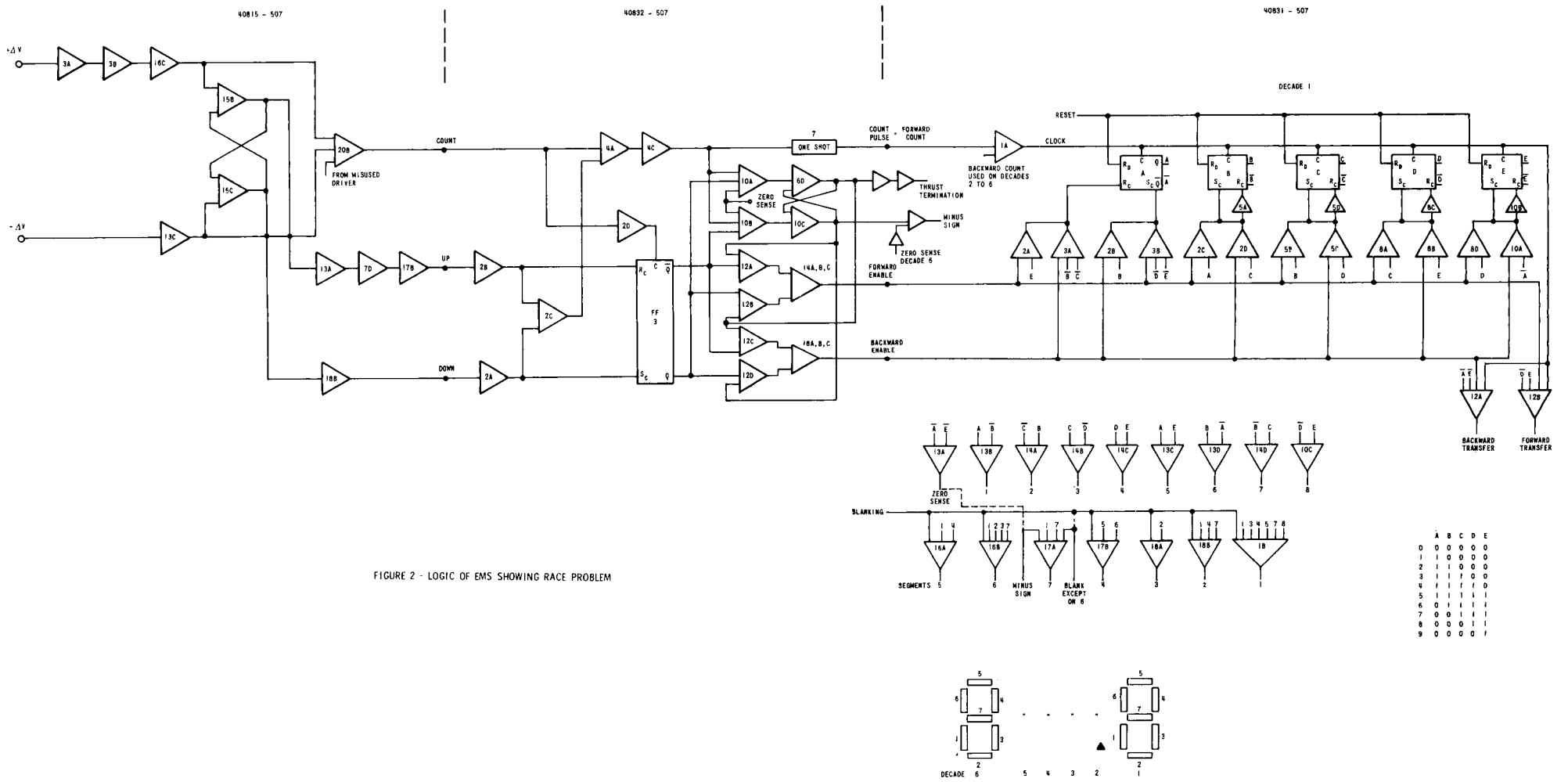


PHOTO BY AUTONETICS, INC.

FIGURE I - ENTRY MONITOR SYSTEM PANEL



	A	B	C	D	E
0	0	0	0	0	0
1	1	0	0	0	0
2	1	1	0	0	0
3	1	1	1	0	0
4	1	1	1	1	0
5	1	1	1	1	1
6	0	1	1	1	1
7	0	0	1	1	1
8	0	0	0	1	1
9	0	0	0	0	1

FIGURE 2 - LOGIC OF EMS SHOWING RACE PROBLEM

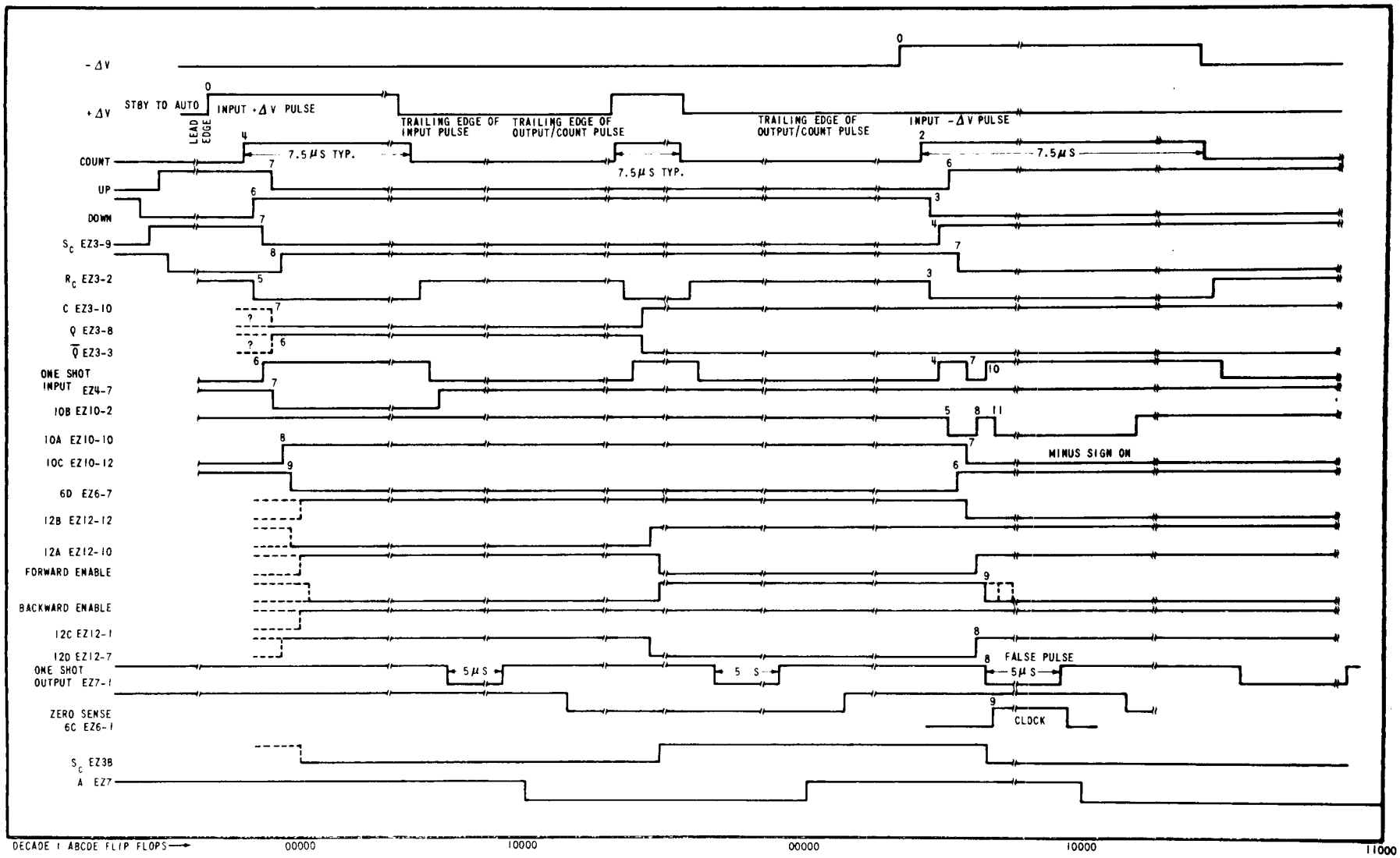


FIGURE 3 - LOGIC RACE

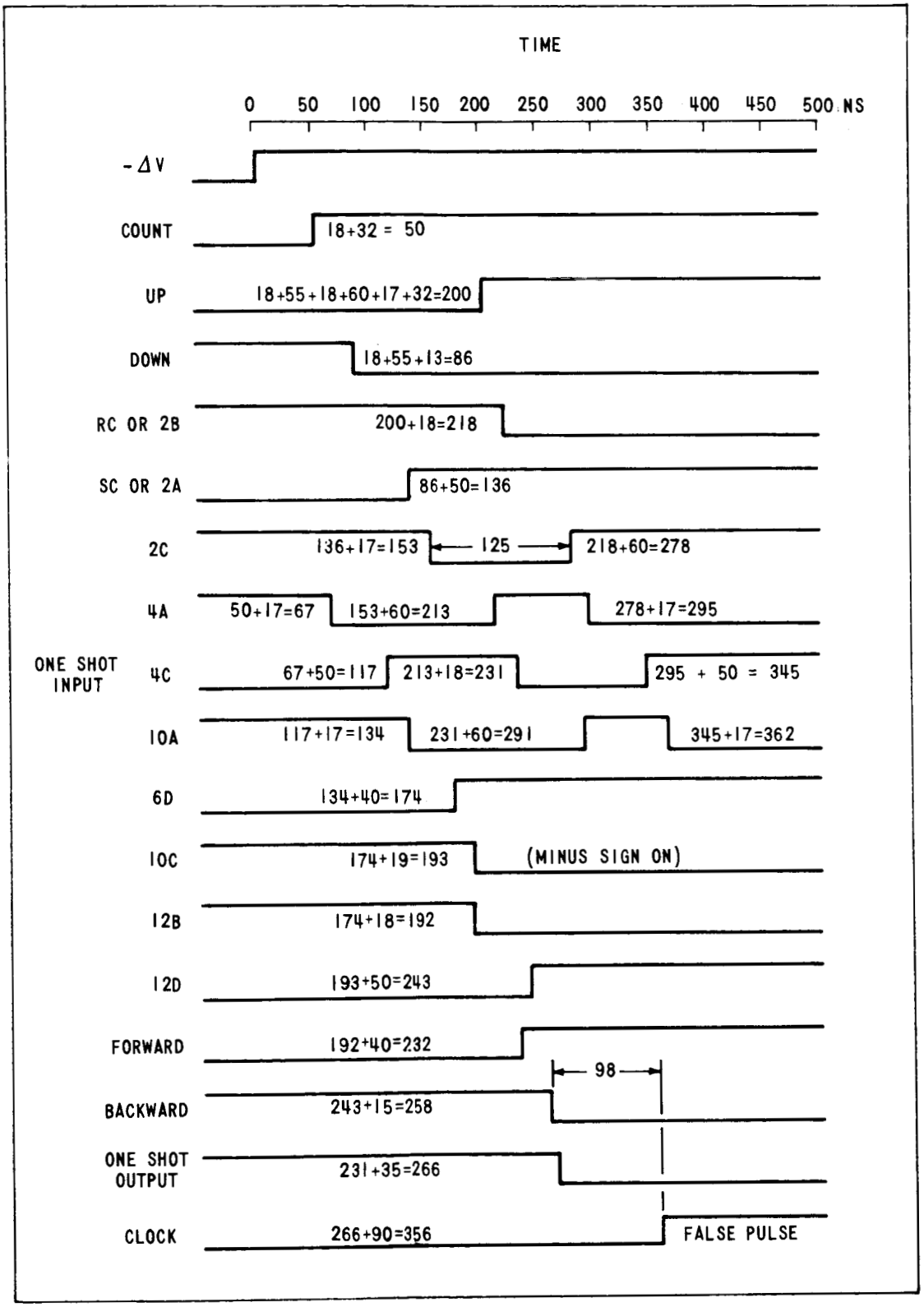


FIGURE 4 - ASSUMING TWO +Δ V PULSES HAVE ENTERED FROM AN INTIAL ALL ZERO CONDITION AND IS FOLLOWED BY A - Δ V PULSE

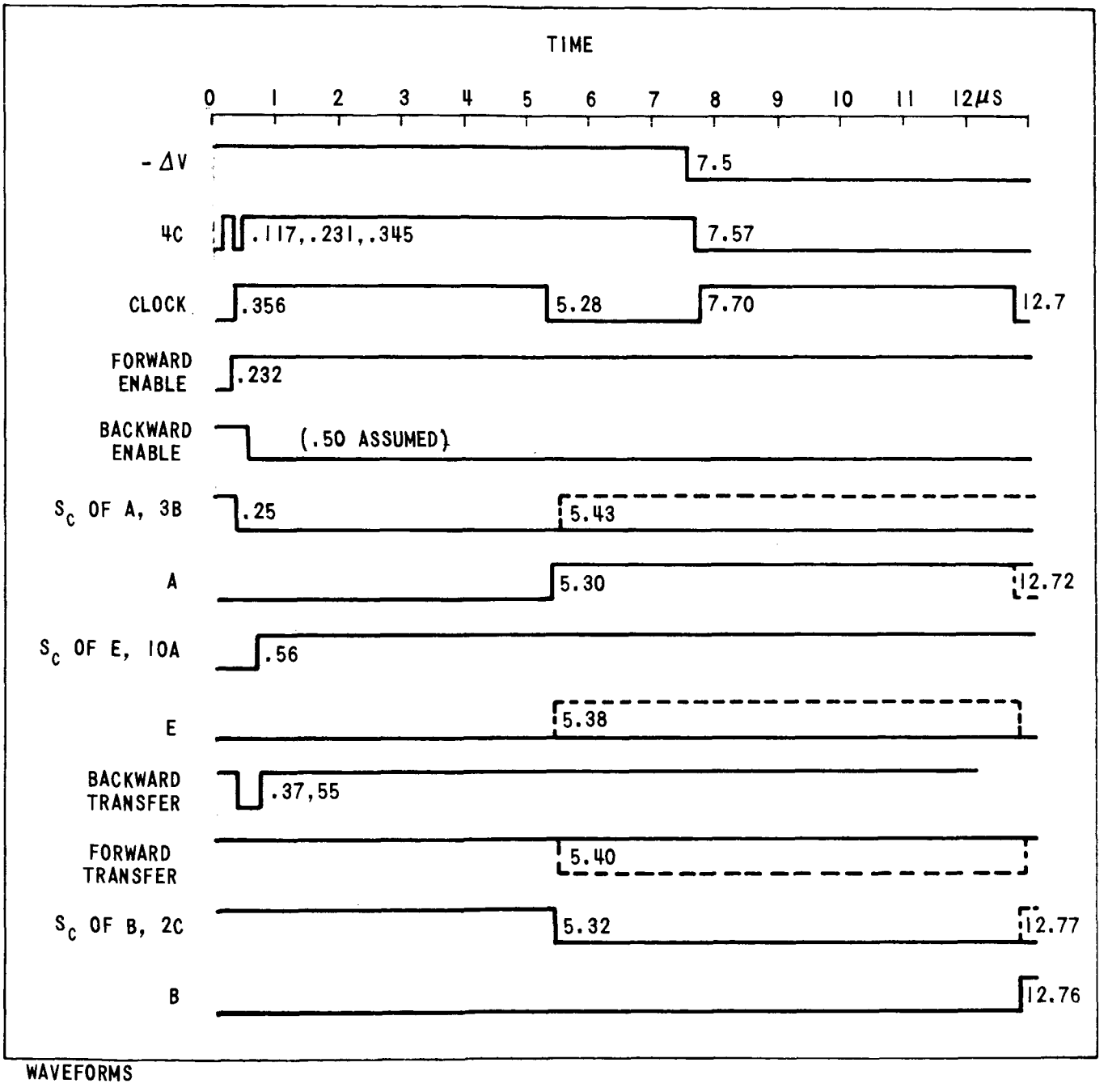


FIGURE 5 - WAVEFORMS SHOWING POSSIBLE JUMP TO -100.

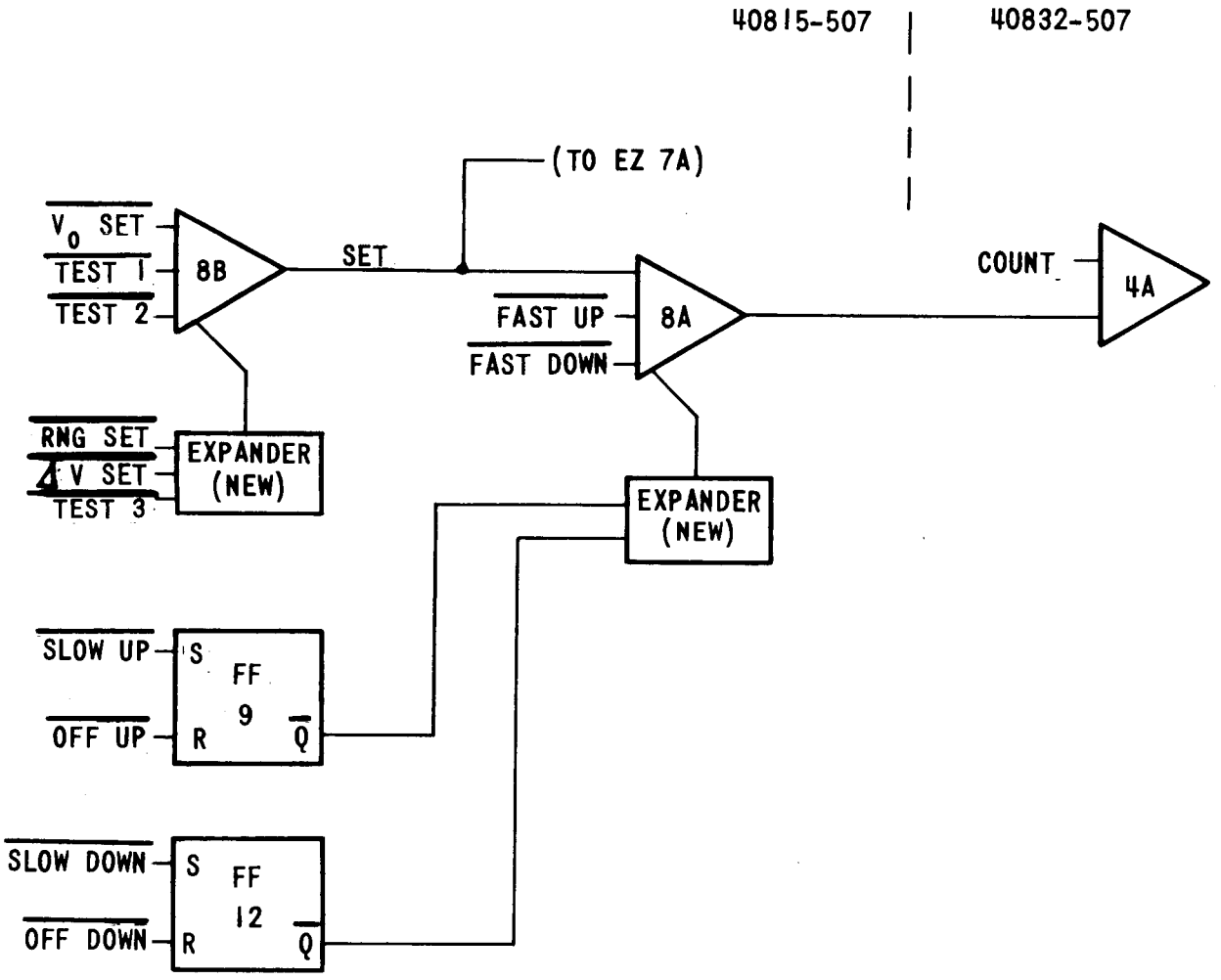


FIGURE 6 - PROPOSED LOGIC FOR COUNT INHIBIT

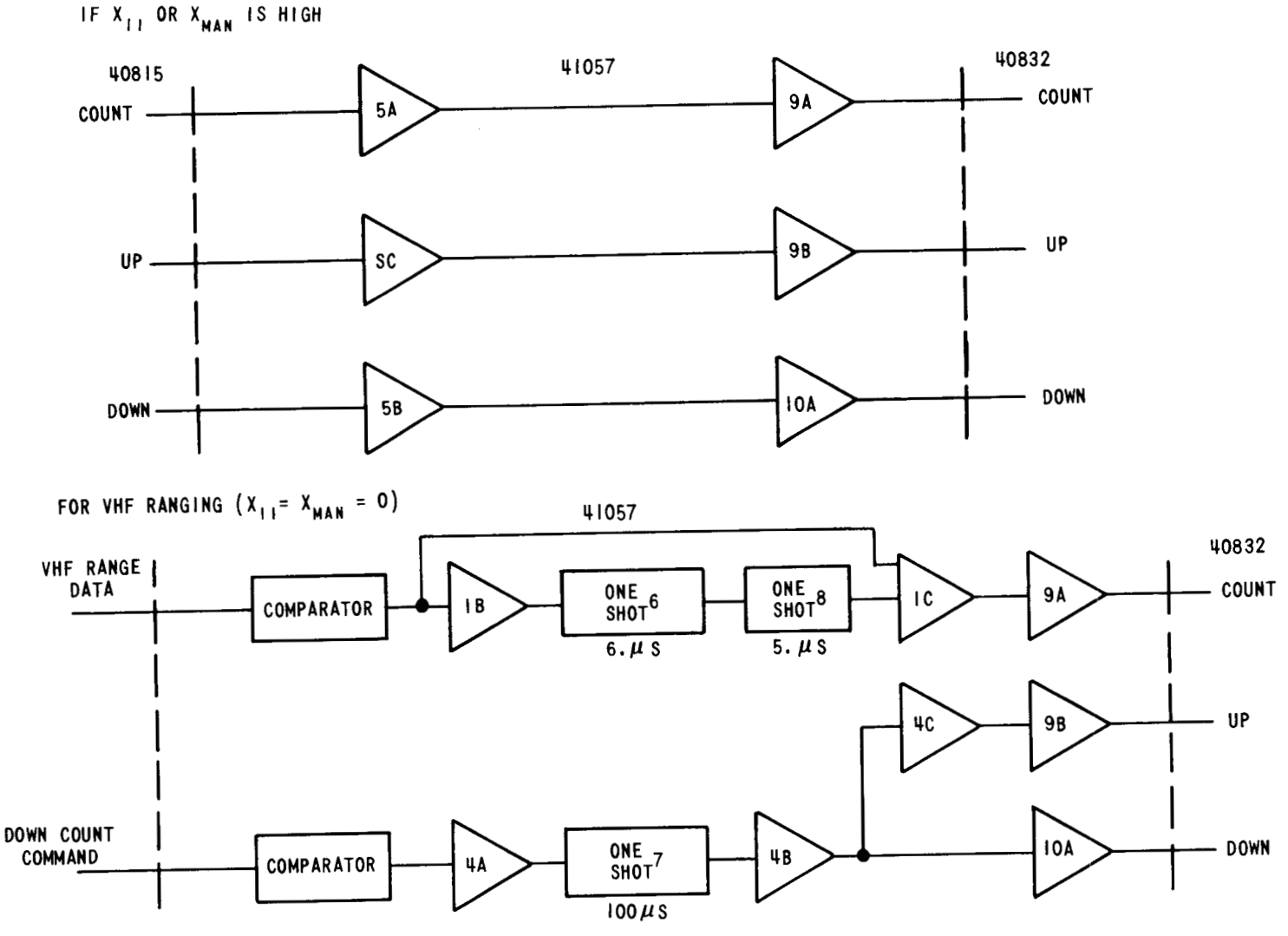


FIGURE 7 - USING VHF RANGING LOGIC

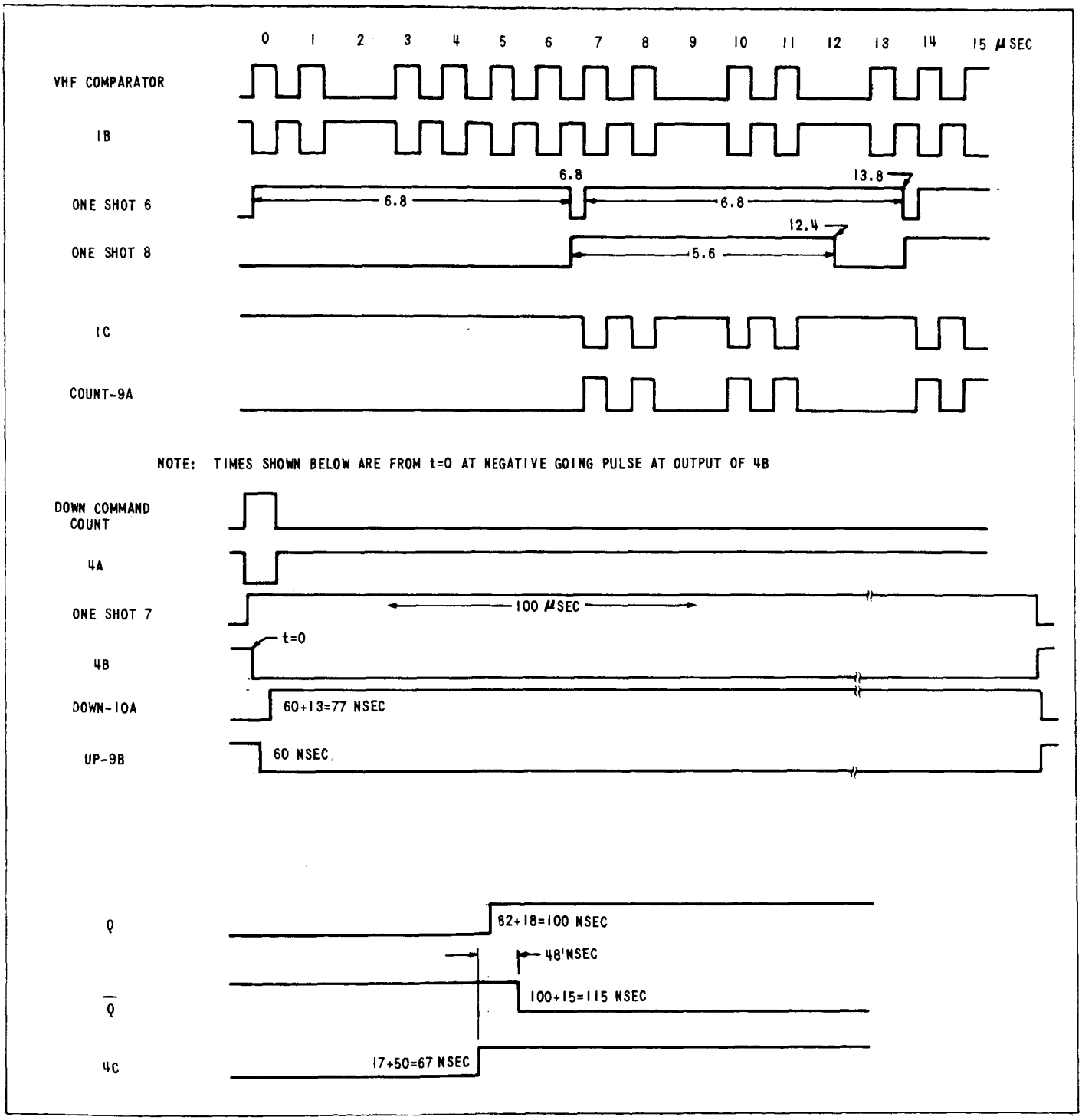
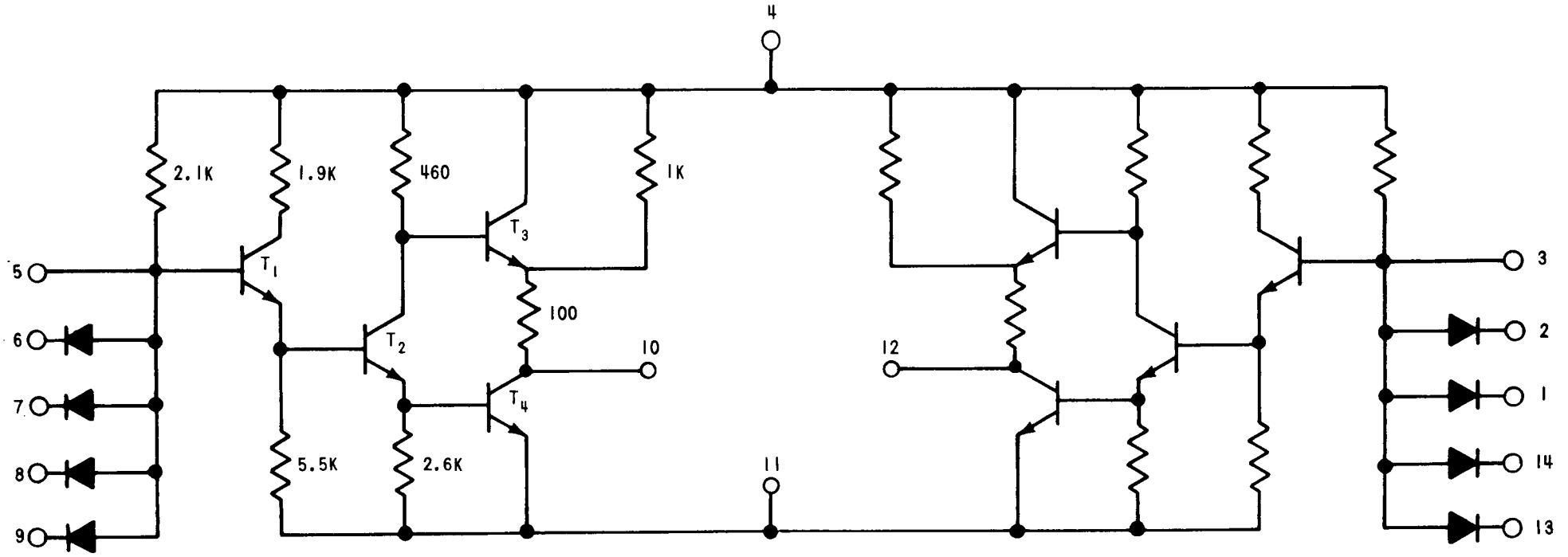
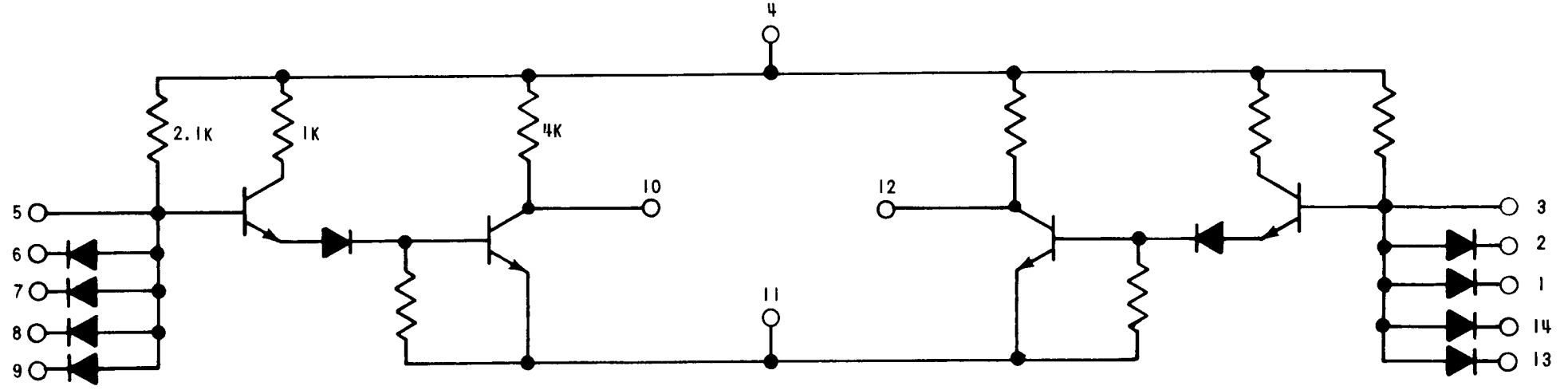


FIGURE 8 - TIMING FOR VHF RANGING

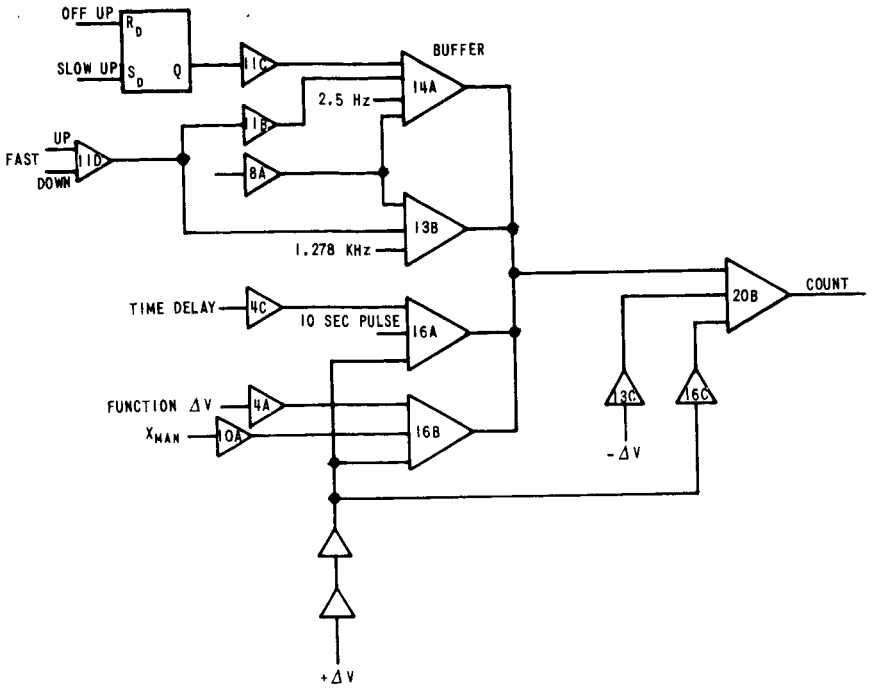


SE156 J DUAL LINE DRIVER

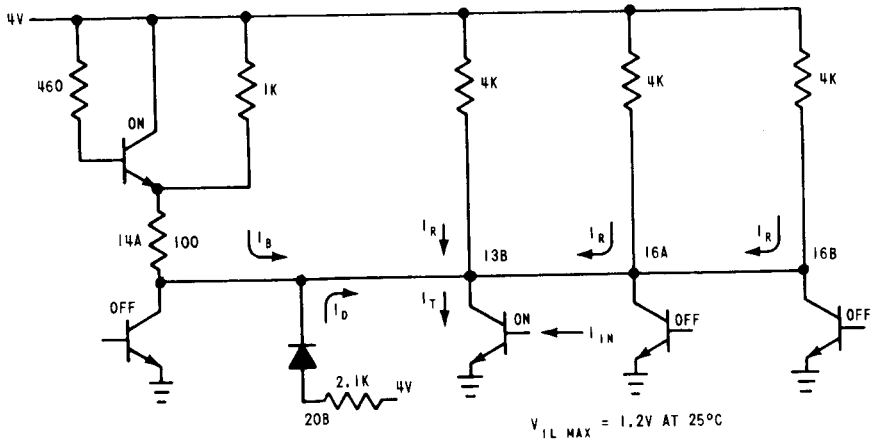


SE116 J DUAL GATE

FIGURE 9 - SIGNETICS NAND GATE AND DRIVER



FOR NOMINAL CASE:



$$I_B = \frac{4-0.7-1.2}{100+460/\beta} + \frac{0.8}{1000} = \frac{2.1}{105} + .008 = 28mA$$

$$I_R = \frac{4-1.2}{4000} = \frac{2.8}{4000} = 0.7mA$$

$$I_D = \frac{4-0.7-1.2}{2100} = \frac{2.1}{2100} = 1.0mA$$

$$I_T = 28 + 3(0.7) + 1 = 31.1mA$$

$$I_{IN} = \frac{4-2.1}{1000} - \frac{0.7}{1800} = 1.9-0.4 = 1.5mA$$

FROM FIGURE 13E OF SIGNETICS DESIGN MANUAL

V_{OL}= 0.63V AT 25°C, V_{NM}<0.57V AND WILL BE WORSE AT HIGHER OR LOWER TEMPERATURE (0°C)

FIGURE 10 - RESULT OF "OR"ing DRIVER OUTPUT